AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A device~~An apparatus~~ comprising:

an upper surface comprising first conductive elements and second conductive elements, the first conductive elements to receive input/output signals from respective conductive elements of an integrated circuit die, and the second conductive elements to receive a first plurality of the input/output signals from respective ones of the first conductive elements; and

a lower surface comprising third conductive elements, the third conductive elements to receive a second plurality of the input/output signals from respective other ones of the first conductive elements.

2. (original) A device according to Claim 1, wherein a first electrical coupling between one of the second conductive elements and a respective one of the first conductive elements comprises a microstripline, and

wherein a second electrical coupling between one of the third conductive elements and a respective other one of the first conductive elements comprises a microvia.

3. (original) A device according to Claim 1, wherein each of the second conductive elements is to receive a respective one of fourth conductive elements, the fourth conductive elements disposed on a first coupling surface of a connector, and

wherein each of the third conductive elements is to receive a respective one of fifth conductive elements, the fifth conductive elements disposed on a second coupling surface of the connector.

4. (original) A device according to Claim 3, wherein the first coupling surface and the second coupling surface face one another.

5. (original) A device according to Claim 3, wherein the fourth conductive elements are connected to conductors within an upper surface of a cable coupled to the connector, and

wherein the fifth conductive elements are connected to conductors within an lower surface of the cable.

6. (original) A device according to Claim 1, the lower surface further comprising:

interface elements to electrically couple the device to a circuit board.

7. (original) A device according to Claim 6, wherein the interface elements are to carry power and ground signals to the integrated circuit die.

8. (original) A device according to Claim 1, wherein a footprint of the first conductive elements is smaller than a footprint of the second conductive elements.

9. (original) A device according to Claim 8, wherein the footprint of the first conductive elements is smaller than a footprint of the third conductive elements.

10. (currently amended) A device comprising:

a first set of conductors electrically couplable to respective ones of first conductive elements of an upper surface of a package, the first set of conductors to receive input/output signals from the first conductive elements;

a second set of conductors electrically couplable to respective ones of second conductive elements of a lower surface of a package, the second set of conductors to receive input/output signals from the second conductive elements; and

a housing to physically couple the first set of conductors to the second set of conductors.

11. (original) A device according to Claim 10, further comprising a middle conductor disposed between the first set of conductors and the second set of conductors.

12. (original) A device according to Claim 11, wherein the middle conductor is electrically isolated from the first set of conductors and from the second set of conductors, and wherein the middle conductor is a ground plane.

13. (original) A device according to Claim 10, further comprising:

a connector comprising:

an upper surface having third conductive elements disposed thereon, the third conductive elements connected to respective ones of the first set of conductors, and to receive respective ones of the first conductive elements; and

a lower surface having fourth conductive elements disposed thereon, the fourth conductive elements connected to respective ones of the second set of conductors, and to receive respective ones of the second conductive elements.

14. (original) A device according to Claim 13, wherein the upper surface and the lower surface face one another.

15. (original) A system comprising:

a package comprising:

an upper surface comprising first conductive elements and second conductive elements, the first conductive elements to receive input/output signals from respective conductive elements of an integrated circuit die, and the second conductive elements to receive a first plurality of the input/output signals from respective ones of the first conductive elements; and

a lower surface comprising third conductive elements, the third conductive elements to receive a second plurality of the input/output signals from respective other ones of the first conductive elements; and

a double data rate memory electrically coupled to the package.

16. (original) A system according to Claim 15, further comprising:

an integrated circuit die comprising die conductive elements, one of the die conductive elements electrically coupled to one of the second conductive elements of the package, and

another one of the die conductive elements electrically coupled to one of the third conductive elements of the package.

17. (original) A system according to Claim 16, further comprising:

a connector comprising:

an upper connector surface having fourth conductive elements disposed thereon, the fourth conductive elements to receive respective ones of the second conductive elements; and

a lower connector surface having fifth conductive elements disposed thereon, the fifth conductive elements to receive respective ones of the third conductive elements; and

a cable comprising a first set of conductors connected to respective ones of the fourth conductive elements and a second set of conductors connected to respective ones of the fifth conductive elements.

18. (original) A system according to Claim 17, further comprising:

a motherboard coupled to the cable and comprising a memory bus, wherein the memory is coupled to the memory bus.

19. (original) A system according to Claim 18, wherein the lower surface of the package comprises interface elements to carry power and ground signals to the integrated circuit die, and wherein

the motherboard is to route the input/output signals to the cable and to route the power and ground signals to the interface elements.

20. (newly-added) A system according to Claim 10, further comprising:

the package,

wherein the upper surface of the package comprises the first conductive elements and third conductive elements, the third conductive elements to receive input/output signals from respective conductive elements of an integrated circuit die, and the first conductive elements to receive a first plurality of the input/output signals from respective ones of the third conductive elements, and

wherein the lower surface of the package comprises the second conductive elements, the second conductive elements to receive a second plurality of the input/output signals from respective other ones of the third conductive elements.

21. (newly-added) A device according to Claim 20, wherein a first electrical coupling between one of the third conductive elements and a respective one of the first conductive elements comprises a microstripline, and

wherein a second electrical coupling between one of the third conductive elements and a respective other one of the second conductive elements comprises a microvia.

22. (newly-added) A device according to Claim 20, the lower surface of the package further comprising:

interface elements to electrically couple the package to a circuit board.

23. (newly-added) A device according to Claim 22, wherein the interface elements are to carry power and ground signals to the integrated circuit die.

24. (newly-added) A device according to Claim 20, wherein a footprint of the third conductive elements is smaller than a footprint of the first conductive elements.

25. (newly-added) A device according to Claim 24, wherein the footprint of the third conductive elements is smaller than a footprint of the second conductive elements.